In the outstanding Office Action, Claim 39 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Claim 62 was rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventors had possession of the claimed invention. Claim 62 was rejected under 35 U.S.C. §103(a) as being unpatentable over Agnello et al. (U.S. Patent No. 5,796,166) or Kasai et al. (IEDM 94-497, pp. 19.4.1 - 19.4.4). Claims 36-42 and 57-61 were rejected under 35 U.S.C. §103(a) as being unpatentable over Agnello et al. or Kasai et al., taken with Fleming et al. (U.S. Patent No. 5,916,634). Claims 38, 41, and 59 were rejected under 35 U.S.C. §103(a) as being unpatentable over Agnello et al. or Kasai et al. taken with Fleming et al., further in view of Wolf et al. ("Silicon Processing for the VLSI ERA"; vol. 2, Lattice Press). Claims 39, 42, and 60 were rejected under 35 U.S.C. §103(a) as being unpatentable over Agnello et al. or Kasai et al. taken with Fleming et al., further in view of Katoh (U.S. Patent No. 5,134,451) Claims 28-35 and 43-56 were rejected under 35 U.S.C. §103(a) as being unpatentable over Sasaki et al. (Jap. Pat. No. 9-260306) or Hah et al. (Jap. Pat. No. 9-186102) taken with Chiang et al. (U.S. Patent No. 5,817,572) and further in view of Fleming et al., and Agnello et al.

Firstly, Applicants' acknowledge with appreciation the courtesy of the Examiner to provisionally set an interview for October 4, 2001, pending filing of a Continued Prosecution Application or the Request for Continued Examination filed herewith.

Secondly, Claim 39 has been amended, without adding new matter, to depend from Claim 37 which provides the antecedent basis for "the gate oxide" in Claim 39. Thus, it is

respectfully submitted that the 35 U.S.C. §112, second paragraph, rejection has been overcome.

Thirdly, Claim 62 has been amended, without adding new matter, to recite at least one of a tungsten nitride layer and a tungsten silicide nitride layer, removing from Claim 62 reference to a tungsten or a tungsten silicide barrier metal. Thus, it is respectfully submitted that the 35 U.S.C. §112, first paragraph, rejection has been overcome.

Briefly, the inventions of Claims 28, 36, 43, 48, 52, 57, 58, and 62 define, respectively, a wiring structure, an electrode, a method of forming a wiring structure, a second method of forming a wiring structure, a third method of forming a wiring structure, a method of forming a gate electrode, a second method of forming a gate electrode, and an electrode of a circuit element. The devices and methods recited include or produce a barrier metal formed of at least one of tungsten nitride WN_x, where x is an atomic fraction of N and comprises a range from 0.5 to 1.0, and tungsten silicide nitride WSi_yN_z, where y is an atomic fraction of Si and comprises a range from 0.01 to 0.2, and z is an atomic fraction of N and comprises a range from 0.02 to 0.2.

Applicants disclose that:

> ...It is therefore possible to prevent the occurrence of segregation and defects. Therefore, the resistance of the via-hole plug 16A and the upper wiring element 16 can be maintained at a low value. In addition, since the adhesiveness does not degrade, it is possible to prevent the metal copper from peeling off.[2]

Applicants further disclose that:

> ... In this case, since the barrier metal 14 of the present invention is interposed between the polysilicon layer 30 and the metal layer 32, it is possible to prevent silicon atoms of the polysilicon layer and metallic atoms

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[2]Specification, page 9, lines 15-21.

of the metal layer 32 from diffusing each other. As a result, it is possible to not only prevent the metal layer 32 from being converted into a silicide but also to prevent formation of pits (vacant holes) that the resistance of the metal layer 32 can be prevented from increasing ans exfoliation of the metal layer 31 can be prevented.[3]

In support of the low sheet resistance and the adhesion of the claimed tungsten nitride WN_x and tungsten silicide nitride WSi_yN_z, alloys, Applicants refer the Examiner to attached Figures 1-5.

Figure 1 shows the relationship between a value x of WN_x and the sheet resistance obtained after a rapid thermal anreal (RTA). Figure 2 shows the relationship between the values, y and z, of WSi_yN_z and the sheet resistance. Figures 1 and 2 depict data for samples whose alloy range is marginally greater than the claimed alloy ranges. The bar chart indicated by "Initial" shows data (sheet resistance) before the heat treatment. The other bar charts show data after the heat treatment.

The sheet resistance of conventional alloys is usually high after a heat treatment. However, the resistance values obtained with the claimed alloys of the present invention are low. Applicants submit that this low resistance indicates that tungsten does not diffuse into the polysilicon layer during the RTA. If tungsten had diffused into the polysilicon layer, the formation of WSi would have generated voids between the tungsten and the polysilicon layer, resulting in a high sheet resistance.

If x, y, z of a tungsten nitride or a tungsten silicon nitride alloy exceed the values shown in Figures 1 and 2, a sheet resistance rapidly increases to several ohms, and often to several tens of ohms. The present inventors consider several ohms to several tens of ohms as

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[3]Specification, page 11, line 24 to page 12, line 9.

high relative to the resistance values shown in the attached Figures 1 and 2. An alloy range of diffusion barriers which do not exhibit after anneal a high sheet resistance has been found for the first time by the present inventors.

Furthermore, Figure 3 is a cross-sectional view of a layer whose x, y, z values fall within a range of tungsten silicon nitride of the present invention. As can be seen form Figure 3, the interface is remarkably planar.

On the other hand, Figure 4 is a cross-sectional view of a tungsten silicon nitride layer whose x, y, z values are outside the range of the present invention. Figure 4 shows that for alloy ranges outside the claimed range of the present invention, tungsten can diffuse into the polysilicon layer, creating a roughened non-planar interface. Furthermore, adhesiveness is damaged in the alloy shown in attached Figure 4 such that it becomes impossible to measure a resistance value for this alloy. Figure 5 shows a W depth profile obtained by secondary ion mass spectroscopy (SIMS) on a W/WN/poly-silicon structure of the present invention, after a RTA. Figure 5 shows that the concentration of W in the polysilicon layer is more than three orders of magnitude lower than the concentration of W in the WN diffusion barrier following the RTA.

Thus, tungsten nitrides and the tungsten silicon nitrides in the claimed ranges of the present invention produce adherent W diffusion barriers capable of preventing W diffusion during RTA, yielding planar interfaces and low sheet resistance electrical contacts.

In the outstanding Office Action, it was stated that "the recitation of the atomic composition of nitrogen in tungsten nitride, and of silicon and nitrogen in tungsten silicon nitride correspond to well known optimization of one skilled in the art to obtain the desired

barrier characteristics and as such would have been obvious."[4] However, as shown in Figures 1 and 4 of Flemming et al. for tungsten silicon and tungsten silicon nitride alloys, the claimed alloy range of the present invention exists outside the experimental region of Flemming et al. Flemming et al. do disclose, in the context of WBN diffusion barriers, WN and W_2N which fall within the claimed range of the present invention. However, Flemming et al. state in discussion of the WBN diffusion barriers that "films with good barrier properties had composition slightly more boron rich than the intersection of the WBN tie line."[5] This suggests that the WN and W_2N films disclosed in Flemming et al. were poor diffusion barriers. Hence, Flemming et al. teach away from the present invention.

Thus, there is no suggestion or motivation in Flemming et al. to deposit the claimed range of diffusion barriers of the present invention. Likewise, Agnello et al., which only disclose a range of TaSiN alloy (Ta between 20% and 40%), do not teach or suggest the claimed range of diffusion barriers of the present invention. No explicit range of tungsten in tungsten nitride layers is disclosed in Kasai et al. or in Hah et al. The other prior art references have been considered, but are deemed no more pertinent, and do not recite the claimed range of diffusion barriers of the present invention or provide motivation or suggestion for one skilled in the art to produce the claimed alloys of the present invention.

Thus, with no disclosure of the claimed range of diffusion barriers defined in independent Claims 28, 36, 43, 48, 52, 57, 58, and 62, and with no suggestion or motivation in the applied prior art to deposit alloys outside the ranges indicated within the prior art

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[4]Office Action, page 4, lines 5-8.

[5] Flemming et al., col. 10, lines 34-37.

references themselves, it is respectfully submitted that Claims 28, 36, 43, 48, 52, 57, 58, and 62 are non-obvious and patentably define over the applied prior art.

Claims 29-35, 37-42, 44-47, 49-51, 53-56, and 59-61 which depend directly or indirectly from independent claims 28, 36, 43, 48, 52, and 57 or 58, respectively, likewise are believed to patentably define over the prior art.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application as amended herewith is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted

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IN THE CLAIMS

Please amend the claims as shown below:

39. (Amended) The electrode according to claim [36] 37, wherein the gate oxide film is formed of any one of SiO_2, SiOF, Ta_2O_5, and CF_x, where x is an atomic fraction of F from 1 to 4.

40. (Amended) A gate electrode of a [translator] transistor formed on a semiconductor substrate, comprising:

a gate oxide film formed between a source and a drain of the transistor;

a barrier metal formed on the gate oxide film; and

a metal layer formed on the barrier metal,

wherein the barrier metal is formed by using CVD of at least one of tungsten nitride WN_x, where x is an atomic fraction of N and comprises a range from 0.5 to 1.0, and tungsten silicide nitride WSi_yN_z, where y is an atomic fraction of Si and comprises a range from 0.01 to 0.2, and z is an atomic fraction of N and comprises a range from 0.02 to 0.2.

62. (Amended) An electrode of a circuit element formed on a semiconductor substrate, comprising:

a polysilicon layer;

a barrier metal formed on the polysilicon layer; and

a metal layer formed on the barrier metal,

wherein the barrier metal comprises at least one of:

[a tungsten layer and] a tungsten nitride layer, and

[a tungsten silicide layer and] a tungsten silicide nitride layer,

and the barrier metal is formed of at least one of tungsten nitride WN_x, where x is an atomic fraction of N and comprises a range from 0.5 to 1.0, and tungsten silicide nitride WSi_yN_z, where y is an atomic fraction of Si and comprises a range from 0.01 to 0.2, and z is an atomic fraction of N and comprises a range from 0.02 to 0.2.